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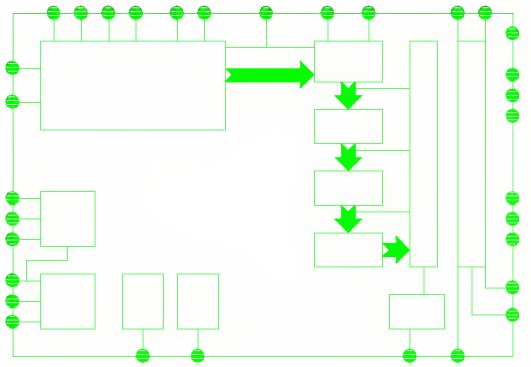
High Speed Oversampling CMOS ADC w/16 Bit Resolution at a 2.5 MHz Output Word Rate

AD9260

FEATURES
Monolithic 16-bit, Oversampled A/D Converter
8X Oversampling Mode, 20 MSPS Clock
2.5MHz Output Word Rate
1.01MHz Signal Passband w/ 0.004 dB Ripple
Signal-to-Noise Ratio: 89dB
Total Harmonic Distortion: -98dB
Spurious Free Dynamic Range: 100dB
Input Referred Noise: 0.6LSB
Selectable Over-Sampling Ratio: 1X, 2X, 4X, 8X
Selectable Power Dissipation: 150mW to 550mW
85dB Stopband Attenuation
0.004dB Passband Ripple
Linear Phase
Single +5V Analog Supply, +5V/+3V Digital Supply
Synchronize Capability for Parallel ADC Interface
Twos-Complement Output Data
44-Pin MQFP



AD9260 BLOCK DIAGRAM

PRODUCT DESCRIPTION

The AD9260 is a 16-bit, high speed oversampled analog-to-digital converter (ADC) that offers exceptional dynamic range over a wide bandwidth. The AD9260 is manufactured on an advanced CMOS process. High dynamic range is achieved with an oversampling ratio of 8X through the use of a proprietary technique which combines the advantages of sigma-delta and pipeline converter technologies.

The AD9260 is a switched-capacitor ADC with a nominal full-scale input range of 4V. It offers a differential input with 60dB of common mode rejection of common mode signals. The signal range of each differential input is +/- 1V centered on a 2.0V common-mode level.

The on-chip decimation filter is configured for maximum performance and flexibility. A series of three half-band FIR filter stages provide 8X decimation filtering with 85 dB of stopband attenuation and 0.004dB of passband ripple. An on-board digital multiplexer allows the user to access data from the various stages of the decimation filter.

The on-chip programmable reference and reference buffer amplifier are configured for maximum accuracy and flexibility. An external reference can also be chosen to suit the users specific dc accuracy and drift requirements.

The AD9260 operates on a single +5V supply, typically consuming 550mW of power. A power scaling circuit is provided allowing the AD9260 to operate at power consumption levels as low as 150mW at reduced clock and data rates. The AD9260 is available in a 44-pin MQFP package and is specified to operate over the industrial temperature range.

PRODUCT HIGHLIGHTS

The AD9260 is fabricated on a very cost effective CMOS process. High-speed, precision mixed-signal analog circuits are combined with high density digital filter circuits.

The AD9260 offers a complete single-chip 16-bit sampling ADC with a 2.5MHz output data rate in a 44-pin MQFP.

Selectable Internal Decimation Filtering - The AD9260 provides a high-performance decimation filter with 0.004dB passband ripple and 85dB of stopband attenuation. The filter is configurable with options for 1X, 2X, 4X, and 8X decimation.

Power Scaling - The AD9260 consumes a low 550mW of power at 16-bit resolution and 2.5MHz output data rate. It's power can be scaled down to as low as 150mW at reduced clock rates.

Single Supply - Both of the analog and digital portions of the AD9260 can operate off of a single +5V supply simplifying system power supply design. The digital logic will also accommodate a single +3V supply for reduced power.

AD9260 - CLOCK INPUT FREQUENCY RANGE

PARAMETER	AD9260	Units
Clock Input (Modulator Sample Rate, FCLOCK)	1	kHz min
	20	MHz max
Decimation Factor (N)	1	min
	8	max
Output Word Rate (FS=FCLOCK/N)	125	Hz min
	20	MHz max

AD9260 - DC SPECIFICATIONS

(AV_{DD}=+5v, DV_{DD}=_3V, DRV_{DD}=+3V, F_{CLOCK}=20MSPS, V_{REF}=2.5V, T_{MIN} to T_{MAX} unless otherwise noted, R_{bias}=2K, Decimation Factor N=8)

PARAMETER	AD9260	Units
RESOLUTION	16	Bits
MAX INPUT SAMPLING RATE	20	MHz
INPUT REFERRED NOISE (V_{REF}=2.5V)	0.6	LSB rms typ
ACCURACY		
Integral Linearity Error	TBD	% FSR
Zero Error	TBD	% FSR
Gain Error (including/excluding internal reference)	TBD	% FSR
TEMPERATURE DRIFT		
Zero Error	TBD	
Gain Error (including/excluding internal reference)	TBD	
POWER SUPPLY REJECTION	TBD	
ANALOG INPUT		
Input Span (with V_{REF}=1.0V)	1.6	Vp-p diff. min
(with V_{REF}=2.5V)	4.0	Vp-p diff. max
Input (Vina or Vinb) Range	+0.5	V min
	+AVDD-0.5	V max
Input Capacitance	15	pF typ
Aperture delay	TBD	ns
Aperture jitter	TBD	ps
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1V mode)	1.0	Volts
Output Voltage Tolerance	TBD	
Output Voltage (2.5V mode)	2.5	Volts
Output Voltage Tolerance (2.5V mode)	TBD	
Load Regulation	1.5	mV
REFERENCE INPUT RESISTANCE	6.4	kΩ typ
POWER SUPPLIES		
Supply Voltages		

AV_{DD}	+5	V (±5% AV_{DD} Operating)
DV_{DD}	+5.25	V max
	+2.7	V min
DRVDD	+5.25	V max
	+2.7	V min
Supply Current		
AV_{DD}	100	mA typ
DV_{DD}	10	mA typ
POWER CONSUMPTION	550	mW typ
	TBD	mW max

AD9260 - AC SPECIFICATIONS

(AV_{DD}=+5V, DV_{DD}=+3V, DRV_{DD}=+3V, f_{CLOCK}=20MSPS, V_{REF}=2.5V, T_{MIN} to T_{MAX} unless otherwise noted, R_{bias}=2K, OSR=8X)

	N=8	N=4	Units
SIGNAL-TO-NOISE RATIO (SNR)	89	82	dB typ
Total Harmonic Distortion (THD)			
fin=100kHz, Ain= -0.2 dBFS	-96		dB typ
fin=100kHz		-98	dB typ
Signal-to-Noise and Distortion Ratio (S/N+D)			
fin=100kHz, Ain= -4.7 dBFS	TBD		dB typ
fin=100kHz		TBD	dB typ
Spurious Free Dynamic Range			
fin=100kHz, Ain= -0.2 dBFS	100		dB typ
fin=100kHz		100	dB typ
Intermodulation distortion			
fin1=475kHz, fin2=525kHz	-95		dB typ
fin1=975kHz, fin2=1.0 MHz		-94	dB typ

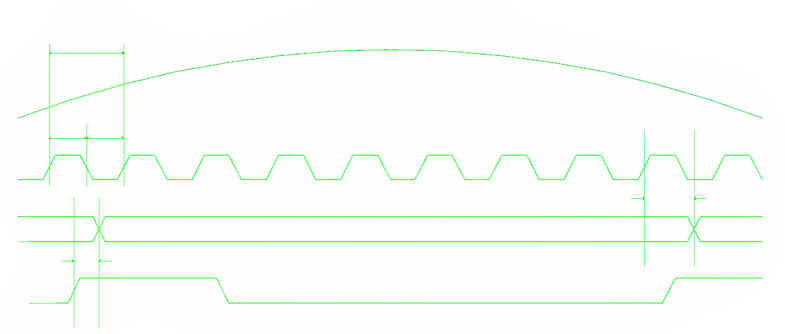
DIGITAL FILTER CHARACTERISTICS

8X Decimation (N=8)			
Passband Ripple	0.004		dB max
Stopband Attenuation	85.5		dB min
Passband	0		MHz min
	1.010*(fCLOCK/20MHz)		MHz max
Stopband	1.490*(fCLOCK/20MHz)		MHz min
	18.510*(fCLOCK/20MHz)		MHz max
Pass-Band/Transition-Band Frequency (-0.1 dB point)	1.074*(fCLOCK/20MHz)		MHz max
(-3dB point)	1.200*(fCLOCK/20MHz)		MHz max
Absolute Group Delay	17.25*(20MHz/fCLOCK)		uS max
Group Delay Variation	0		uS max
Settling Time (to +/- 0.0007%)	15.60*(20MHz/fCLOCK)		us max
4X Decimation (N=4)			
Passband Ripple	0.003		dB max
Stopband Attenuation	85.5		dB min
Passband	0		MHz min

	1.890*(fCLOCK/20MHz)	MHz max
Stopband	3.120*(fCLOCK/20MHz)	MHz min
	16.88*(fCLOCK/20MHz)	MHz max
Pass-Band/Transition-Band Frequency (-0.1 dB point)	2.049*(fCLOCK/20MHz)	MHz max
(-3dB point)	2.389*(fCLOCK/20MHz)	MHz max
Absolute Group Delay	5.45*(20MHz/fCLOCK)	uS max
Group Delay Variation	0	uS max
Settling Time (to +/- 0.0007%)	5.60*(20MHz/fCLOCK)	us max
2X Decimation (N=2)		
Passband Ripple	0.0005	dB max
Stopband Attenuation	85.5	dB min
Passband	0	MHz min
	2.491*(fCLOCK/20MHz)	MHz max
Stopband	7.519*(fCLOCK/20MHz)	MHz min
	12.481*(fCLOCK/20MHz)	MHz max
Pass-Band/Transition-Band Frequency (-0.1 dB point)	3.231*(fCLOCK/20MHz)	MHz max
(-3dB point)	4.535*(fCLOCK/20MHz)	MHz max
Absolute Group Delay	1.15*(20MHz/fCLOCK)	uS max
Group Delay Variation	0	uS max
Settling Time (to +/- 0.0007%)	1.30*(20MHz/fCLOCK)	us max

DIGITAL SPECIFICATIONS (AV_{DD}=+5V, DV_{DD}=+5V, T_{MIN} to T_{MAX} unless otherwise noted)

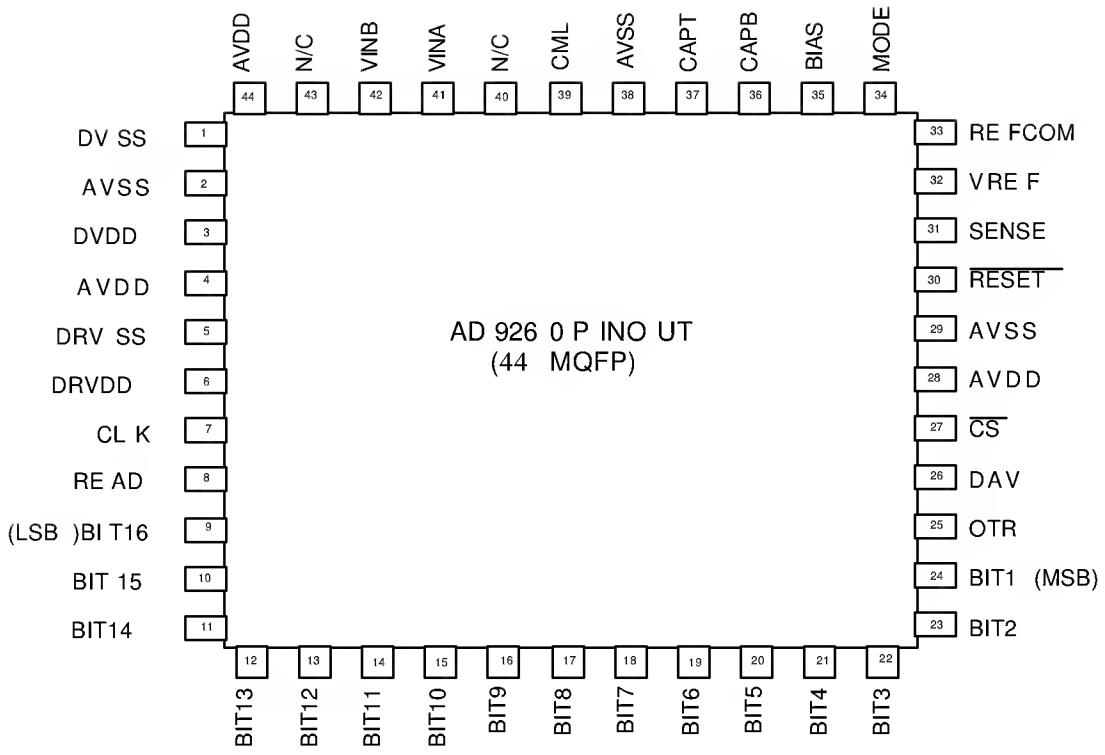
PARAMETER	AD9260	Units
LOGIC INPUTS		
High Level Input Voltage	+3.5	V min
Low Level Input Voltage	+1.0	V max
High Level Input (Current (V_{IN}=DV_{DD})	+/–10	µA max
Low Level Input Current (V_{IN}=0V)	+/-10	µA max
Input Capacitance	5	pF typ
LOGIC OUTPUTS (with DRV_{DD}=5V)		
High Level Output Voltage (I_{OH}=50 µA)	+4.5	V min
High Level Output Voltage (I_{OH}=0.5 mA)	+2.4	V min
Low Level Output Voltage (I_{OL}=1.6 mA)	+0.4	V max
Low Level Output Voltage (I_{OL}=50 µA)	+0.1	V max
Output Capacitance	5	pF typ
LOGIC OUTPUTS (with DRV_{DD}=3V)		
High Level Output Voltage (I_{OH}=50 µA)	+2.4	V min
Low Level Output Voltage (I_{OL}=50 µA)	+0.7	V max



AD9260 Timing Diagram

SWITCHING SPECIFICATIONS (AV_{DD}=+5V, DV_{DD}=+5V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	Symbol	AD9260	Units
Clock Period	tc	50	ns min
Clock Pulse Width High	tch	25	ns min
Clock Pulse Width Low	tcl	25	ns min
Data Hold Time	th	3.5	ns min
Output Delay	tod		ns min



PIN DESCRIPTION

Name	Description	MQFP
CLK	Clock Input Pin	7
READ	Part of DSP interface - pull low to disable output bits	8
Bit 16	Least Significant Data Bit (LSB)	9
Bit N	Data Output Bit	10-23
Bit 1	Most Significant Data Bit (MSB)	24
OTR	Out of Range - set when converter or filter overflows	25
AVDD	+5V Analog Supply	4,28,44
AVSS	Analog Ground	2,29,38
SENSE	Reference Amplifier SENSE: selects REF level	31
VREF	Input Span Select Reference I/O	32
REFCOM	Reference Common	33
CAPB	Noise Reduction Pin - Decouples Reference Level	36
CAPT	Noise Reduction Pin	37
CML	Common Mode Level (AVDD/2.5)	39
VINA	Analog Input Pin (+)	41
VINB	Analog Input Pin (-)	42
DVSS	Digital Ground	1
DVDD	+3 to +5 V Digital Supply	3
DRVSS	Digital Output Driver Ground	5
DRVDD	+3 to +5 V Digital Output Driver Supply	6
N/C	No Connect (ground for shielding purposes)	43,40
DAV	Data Available	26
$\overline{CS}$	Chip Select (CSB): Active LOW	27
$\overline{RESET}$	RESETB: Active LOW	30
MODE	Mode Select - selects decimation mode	34
BIAS	Power Bias	35

PERFORMANCE CHARACTERIZATION CURVES

Figure A : A spectral plot of the AD9260 at 100kHz input, 20MHz clock, 8X OSR (2.5MHz output data rate)

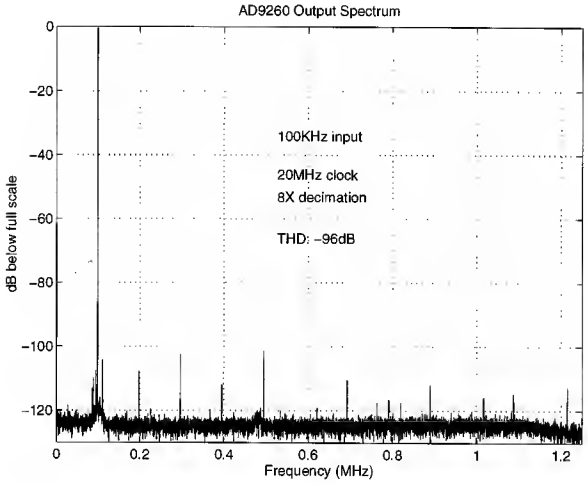


Figure A

Figure B: A spectral plot of the AD9260 at 100kHz input, 20MHz clock, 4X OSR (5 MHz output data rate)

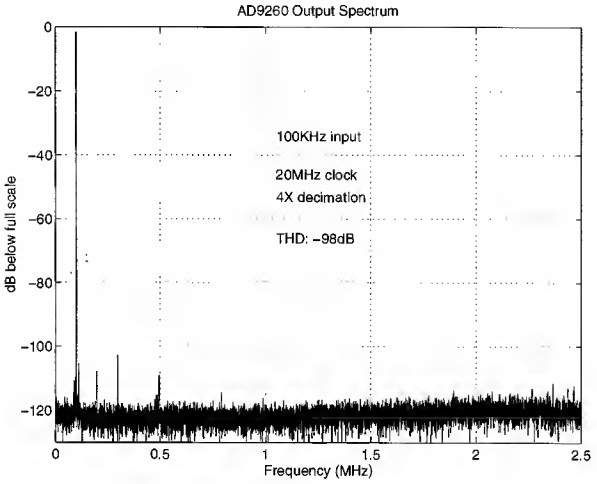


Figure B

Figure C: A spectral plot of the AD9260 at 100kHz input, 20MHz clock, 2X OSR (10 MHz output data rate)

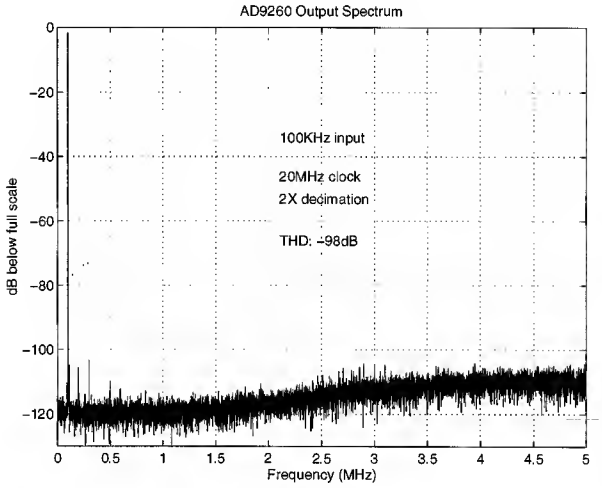


Figure C

Figure D: A spectral plot of the AD9260 at 100kHz input, 20MHz clock, Undecimated (20MHz output data rate)

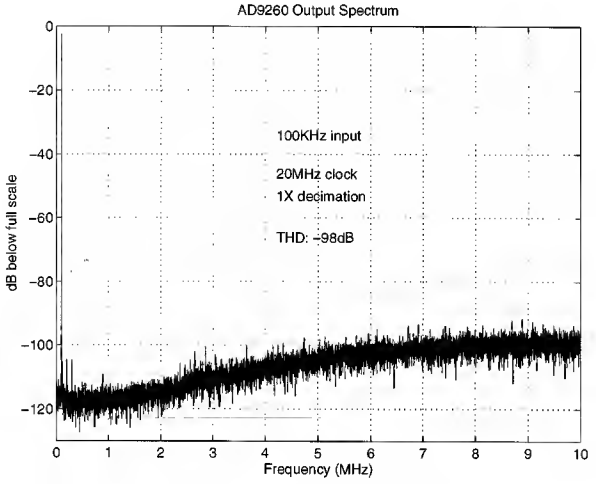


Figure D

Figure E: SFDR & SDR vs. input amplitude for 100kHz input. SNR vs. input amplitude for 1MHz input.

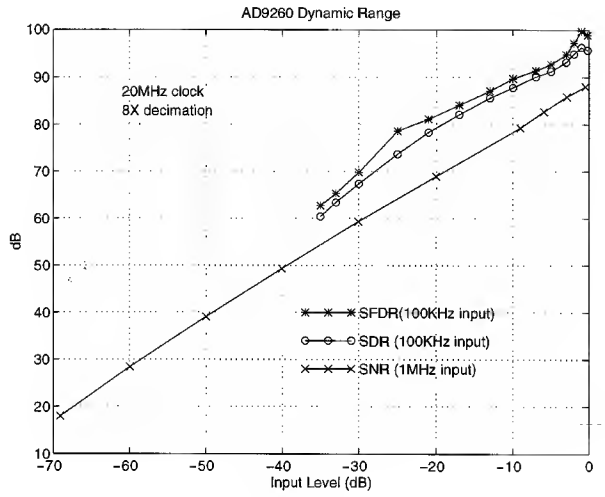


Figure E

Figure F: Two tone spectral performance of the AD9260 given inputs at 975kHz and 1.0 MHz, 20MHz clock, 8X decimation

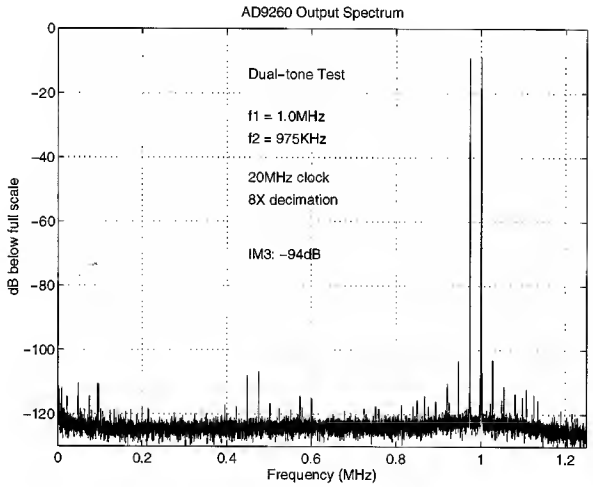


Figure F

THEORY OF OPERATION

The AD9260 utilizes a new analog-to-digital converter architecture to combine sigma-delta techniques with a high speed, pipelined A/D converter. This topology allows the AD9260 to offer the high dynamic range associated with sigma-delta converters while maintaining very wide input signal bandwidth (1.25MHz) at a very modest 8X oversampling ratio. Figure 2 provides a block diagram of the AD9260. The differential analog input is fed into a 2nd order, multi-bit sigma delta modulator. This modulator features a 5 bit flash quantizer and 5 bit feedback. In addition, a 12 bit pipelined A/D quantizes the input to the 5-bit flash to greater accuracy. A special digital modulation loop combines the output of the 12 bit pipelined A/D with the delayed output of the 5 bit flash to produce the equivalent response of a 2nd order loop with a 12 bit quantizer and 12 bit feedback. The combination of a 2nd order loop and multi-bit feedback provide inherent stability: the AD9260 is not prone to idle tones or full-scale idiosynchrocies sometimes associated with higher order single bit sigma-delta modulators.

The output of this 12 bit modulator is fed into the digital decimation filter. The voltage level on the MODE pin establishes the configuration for the digital filter. The user may bring the data out undecimated (at the clock rate), or at a decimation factor of 2X, 4X, or a full 8X. The spectra for these 4 cases are shown in figures A,B,C, and D, all for a 100kHz full scale input and 20MHz clock. The spectra of the undecimated output clearly shows the 2nd order shaping characteristic of the quantization noise as it rises at frequencies above 1.25MHz. The on-chip decimation filter provides excellent stop band rejection to suppress any stray input signal between 1.25MHz and 18.75MHz, substantially easing the requirements on any anti-aliasing filter for the analog input path. The decimation filters are integrated with symmetric FIR filter structures, providing a linear phase response and excellent passband flatness.

The digital output driver register of the AD9260 features both READ and CHIP SELECT pins to allow easy interfacing. The digital supply of the AD9260 is designed to operate over a 2.7 to 5.25 V supply range, though 3V supplies are recommended to minimize digital noise on the board. A DATA AVAILABLE pin allows the user to easily synchronize to the converter's decimated output data rate. OUT-OF-RANGE (OTR) indication is given for an overflow in the pipelined A/D converter or digital fiters. A RESETB function is provided to synchronize the converter's decimated data and clear any overflow condition in the analog integrators.

An on-chip reference and reference buffer are included on the AD9260. The reference can be configured in either a 2.5V mode (providing a 4V pk-

pk differential input full scale), a 1V mode (providing a 1.6V pk-pk differential input full scale), or programmed with an external resistor divider to provide any voltage level between 1V and 2.5V.

For users wishing to operate the part at reduced clock frequencies, the bias current of the AD9260 is designed to be scalable. This scaling is accomplished through use of the proper external resistor tied to the BIAS pin: the power can be reduced roughly proportionately to clock frequency by as much as 75% (for clock rates of 5MHz).

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 1, a simplified model of the AD9260, highlights the relationship between the analog inputs, VINA, VINB, and the reference voltage VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the A/D converter. An internal reference buffer in the AD9260 scales the reference voltage VREF before it is applied internally to the AD9260 *A/D core*. The scale factor of this reference *buffer* is 0.8. Consequently, the maximum input voltage to the *A/D core* is +0.8×VREF. The minimum input voltage to the A/D core is automatically defined to be -0.8×VREF. With this scale factor, the maximum differential input span of 4Vp-p is obtained with a VREF voltage of 2.5V. A smaller differential input span may be obtained by using a VREF voltage of less than 2.5V. The distortion performance of the AD9260 improves with a smaller input span, while the noise performance degrades.

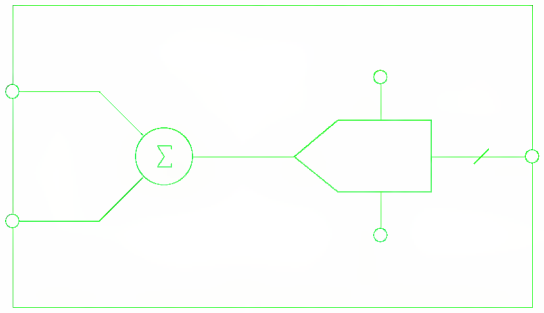


Figure 1: AD9260 Simplified Input Model

INPUT SPAN

The AD9260 is implemented with a differential input structure. This structure allows the common-mode level (average voltage of the two input pins) of the input signal to be varied independently of the input span of the converter. Specifically, the input to the *A/D core* is the difference of the voltages applied at the VINA and VINB input pins. Therefore, the equation,

(1) V_{CORE} = VINA-VINB

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

(2) $-0.8 \times VREF <= V_{CORE} <= +0.8 \times VREF$

where VREF is the voltage at the VREF pin.

INPUT COMPLIANCE RANGE

In addition to the limitations on the differential span of the input signal indicated in equation 2, there is an additional limitation placed on the inputs by the analog input structure of the AD9260. The analog input structure bounds the valid operating range for VINA and VINB. The condition,

(3) AVSS < VINA < AVDD - 1.0V
AVSS < VINB < AVDD + 1.0V

where AVSS is nominally 0V and AVDD is nominally +5V, defines this requirement. Thus the valid inputs for VINA and VINB is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationships between VINA, VINB, VREF and the digital output of the AD9260, see Table II.

Refer to Table I. for a summary of the various analog input and reference configurations.

ANALOG INPUT OPERATION

The analog input structure of the AD9260 is optimized to meet the performance requirements for some of the most demanding communication and data acquisition applications. This input structure is composed of a switched-capacitor network which samples the input signal applied to pins VINA and VINB on every rising edge of the CLK pin. The

input switched capacitors are charged to the input voltage during each period of CLK. The resulting charge, q, on these capacitors is equal to C×Vin, where C is the input capacitor. The change in charge on these capacitors, delta q, as the capacitors are charged from a previous sample of the input signal to the next sample is approximated in the following equation,

$$\textbf{(4) delta q} \sim C \times \text{deltaV}_N = C \times (V_N - V_{N-2})$$

where V_N represents the present sample of the input signal and V_{N-2} represents the sample taken two clock cycles earlier. The average current flow into the input (provided from an external source) is given in the following equation,

$$\textbf{(5) } I = \text{delta } q/T \sim C \times (V_N - V_{N-2}) \times F_{CLOCK}$$

where T represents the period of CLK and F_{CLOCK} represents the frequency of CLK. Equations 4 and 5 provide simplifying approximations of the operation of the analog input structure of the AD9260. A more exact, detailed description and analysis of the input operation is provided below.

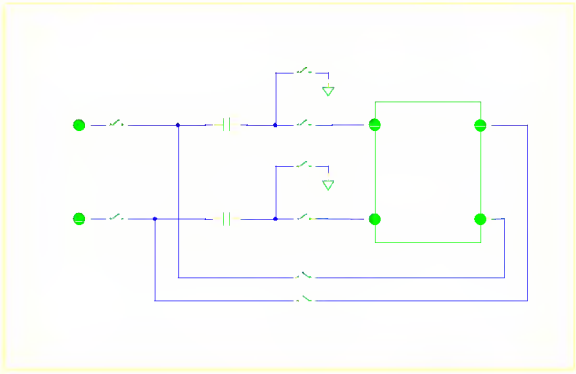


Figure 2: AD9260 Analog Input Structure

Figure 2 illustrates the analog input structure of the AD9260. The switched capacitors, *CS1* and *CS2*, sample the input voltages applied on pins VINA and VINB. These capacitors are connected to input pins VINA and VINB when CLK is low. When CLK rises a sample of the input signal is taken on capacitors *CS1* and *CS2*. When CLK is high, capacitors *CS1* and *CS2* are connected to the *Analog Modulator*. The modulator pre-charges capacitors *CS1* and *CS2* to minimize the amount of charge required from any circuit used in combination with the AD9260 to drive input pins VINA and VINB. This reduces the input drive requirements of the analog circuitry driving pins VINA and VINB. The *Analog Modulator* pre-charges the voltages across capacitors *CS1* and *CS2* approximately equal to a delayed version of the input signal. When capacitors *CS1* and *CS2* are connected to input pins VINA and VINB, the differential charge, Q(n), on these capacitors is given in the following equation,

$$\textbf{(6) } Q(n) = q1 - q2 = CS \times V_{CORE}$$

where q1 and q2 are the individual charges stored on capacitors *CS1* and *CS2* respectively, and CS is the capacitance value of *CS1* and *CS2*. When capacitors *CS1* and *CS2* are connected to the *Analog Modulator* during the preceding "pre-charge" clock phase, the capacitors are pre-charged equal to an approximation of a previous sample of the input signal. Consequently the differential charge on these capacitors while CLK is high is given in the following equation,

$$\textbf{(7) } Q(n-1) = CS \times V_{CORE(delay)} + CS \times \text{Vdelta}$$

where $V_{CORE(delay)}$ is the value of VCORE sampled during a previous period of CLK, and Vdelta is the sigma-delta error voltage left on the capacitors. Vdelta is a natural artifact of the sigma-delta feedback techniques utilized in the *Analog Modulator* of the AD9260. It is a small random voltage term which changes every clock period and varies from 0 to +/- 0.05*Vref.

The analog circuitry used to drive the input pins of the AD9260 must respond to the charge glitch which occurs when capacitors CS1 and CS2 are connected to input pins VINA and VINB. This circuitry must provide additional charge, qdelta, to capacitors CS1 and CS2 which is the difference between the pre-charged value, Q(n-1), and the new value, Q(n), as given in the following equation,

$$\textbf{(8) } Qdelta = Q(n) - Q(n-1)$$

$$\textbf{(9) } Qdelta = CS \times [V_{CORE} - V_{CORE(delay)} + \text{Vdelta}]$$

The term $V_{CORE(delay)}$ in equation 9 represents the value of V_{CORE} exactly 2 periods of CLK prior to the instant V_{CORE} is sampled on *CS1* and *CS2*. For example, if a 20MHz CLK frequency (50ns period) is applied to the AD9260, then the delay is 2

periods×50ns/period = 100ns. In this example, if the input signal is a 100kHz sine wave with 2V amplifude, then the worst-case slope of the input signal, dV/dt, is $A \times 2 \times p \times f = 2 \times 2 \times 3.1416 \times 1e5$ = 1.27mV/ns. In this example there is a delay of 100ns between the two samples of the input signal, and therefore the value of V_{CORE} -$V_{CORE(delay)}$ <= 1.27mV/ns × 100ns = 127mV. The Vdelta term in equation 9 also contributes to the charge. For example, if VREF = 2.5V, then Vdelta varies from 0 to VREF×0.05 = 125mV. Therefore, the value of Qdelta in this example ranges from 0 to CS×(127mV+125mV) = CS×252mV.

The analog input structure for the AD9260 provides superior linearity, high-frequency distortion performance, and wide-band noise performance. The performance of this input structure is achieved, in part, due to the use of a switched-capacitor circuit which is not offset compensated. A consequence of this circuit implementation is that the DC offset of the AD9260 is typically in the range of 0 to 2mV.

The charge glitch in the example above is much lower than the charge glitch of a conventional switched-capacitor input structure. In the conventional input structure the input capacitors are not pre-charged. Therefore all of the charge in capacitors CS1 and CS2 must be provided every clock period. In the example above the input signal has a 2V amplitude, and therefore the corresponding value of Qdelta for a conventional input structure is CS×2V. Therefore in this example the input structure of the AD9260 provides a 7.9X (2/.252) reduction of charge glitch.

The pre-charging technique in the AD9260 is most effective for low frequency input signals in which the value of $V_{CORE(delay)}$ is very close to the value of V_{CORE}. For high frequency input signals (e.g. 1MHz) the technique is less effective. In the example above, if the input frequency is changed to 1MHz, then the value of Qdelta ranges from 0 to CS×(1.27V + 125mV) = CS×1.4V. which is a 1.4× (2/1.4) reduction of charge glitch as compared to that of a conventional input structure.

DRIVING THE INPUT

Transient Response

The charge glitch occurs once at the beginning of every period of the input CLK (falling edge), and the sample is taken on capacitors *CS1* and *CS2* exactly one-half period later (rising edge). Figure 3 presents a typical input waveform applied to input pins VINA and VINB of the AD9260.

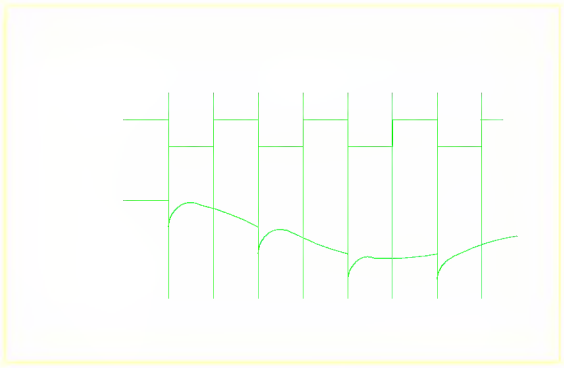


Figure 3: AD9260 Typical Input Waveform

This figure illustrates the effect of the charge glitch when a source with non-zero output impedance is used to drive the input pins. This source must be capable of settling from the charge glitch in one-half period of the CLK. Unfortunately, the MOS switches used in any CMOS switched capacitor circuit (including those in the AD9260) include non-linear parasitic junction capacitances connected to their terminals. Figure 4 provides a more detailed representation of the analog input structure of the AD9260 which further illustrates the parasitic capacitances, Cpa1, Cpb1, Cpa2, and Cpb2, associated with the input switches.

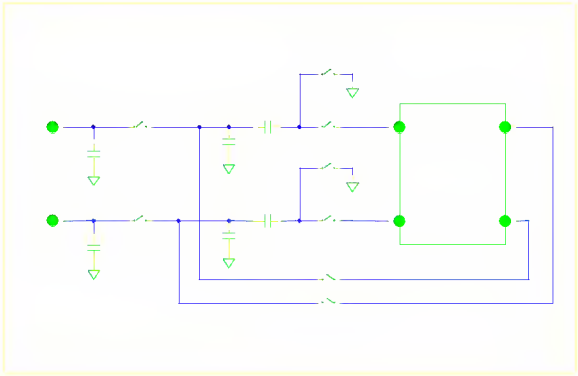


Figure 4: AD9260 Detailed Analog Input Structure

Parasitic capacitor Cpa1 and Cpa2 are always connected to pins VINA and VINB and therefore do not contribute to the glitch energy. Parasitic capacitors Cpb1 and Cpb2, on the other hand, cause a charge glitch which adds to that of input capacitors

CS1 and CS2 when they are connected to input pins VINA and VINB. The non-linear junction capacitance of Cpb1 and Cpb2 cause charge glitch energy which is non-linearly related to the input signal. Therefore, linear settling is difficult to achieve unless the input source completely settles during one-half period of CLK. A portion of the glitch impulse energy "kicked" back at the source is not linearly related to the input signal. Therefore the best way to insure that the input signal settles linearly is to use wide-bandwidth circuitry which settles as completely as possible from the glitch during one-half period of the CLK.

The AD9260 utilizes a proprietary clock-boosted boot-strapping technique to reduce the nonlinear parasitic capacitances of the internal CMOS switches. This technique improves the linearity of the input switches and reduces the non-linear parasitic capacitance. Thus, this technique reduces the nonlinear glitch energy. The capacitance values for the input capacitors and parasitic capacitors for the input structure of the AD9260, as illustrated in Figure 4, are listed as follows:
CS = 3.2pF, Cpa=6pF, Cpb = 1pF (where CS is the capacitance value of capacitors CS1 and CS2, Cpa is the value of capacitors Cpa1 and Cpa2, and Cpb is the value of capacitors Cpb1 and Cpb2). The total capacitance at each input pin is Cin = CS+Cpa+Cpb=10.2pF.

AC Response

The optimum distortion performance is achieved with the input common-mode voltage (average voltage of the two input pins VINA and VINB) set equal to AVDD/2.5. For example with a 5V analog supply the optimum common-mode level of the input signal is 2V. A pair of series isolation resistors, *RI1* and *RI2*, inserted between the *analog input drive circuitry* and input pins VINA and VINB as shown in Figure 5, provides effective isolation of the input source from the charge glitch.

In Figure 5 the *analog input drive circuitry* is implemented using two wide-band low-noise buffers that absorb the charge glitch from the AD9260. These wide-bandwidth buffers may be implemented, for example, as shown on the AD9260 evaluation board with two emitter followers. Selection of buffers with >85dB THD at 1MHz is recommended to avoid performance limitations due to buffer non-linearity.

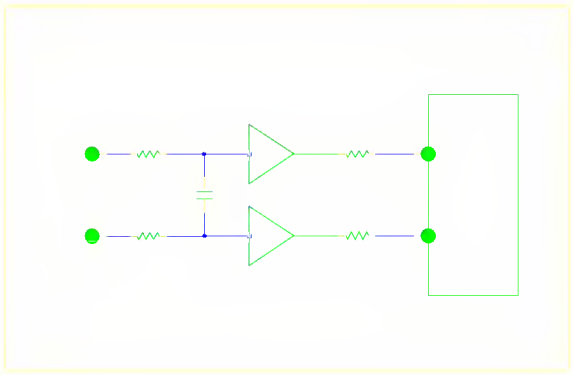


Figure 5: AD9260 Analog Input Drive Circuitry

The optimum values of resistors *RI1* and *RI2* depends on several factors including the AD9260 sample rate, the *analog input drive circuitry*, and the particular application. For optimal distortion performance resistors *RI1* and *RI2* should be chosen to maintain a time constant, tau = Rin*Cin = Thalf/10, where Thalf is one-half the period of CLK. For example, with a 20MHz CLK, the tau should be maintained less than 2.5ns for optimal distortion performance. This corresponds to a resistor value of less than 250Ω.

Noise

The optimum noise performance is achieved with the largest input signal voltage span (i.e. 4V input span). Great care should be taken to minimize the noise of the input source. A transformer coupled passive input circuit should be considered for obtaining the lowest noise performance. Most commercially available op-amps which are capable of driving the inputs of the AD9260 with wide-enough bandwidth to achieve optimal distortion performance typically limit the overall noise performance. To help reduce the input noise an RC filter (resistors *RF1*, *RF2*, and *CF*) may be used as shown in Figure 5. This RC filter in Figure 5 is isolated from the charge glitch of the AD9260 by the wide-bandwidth buffers. For this reason the bandwidth of the RC filter may be reduced below the frequency of the CLK signal in order to remove wide-band noise from any analog circuitry in the signal path preceding the *analog input drive circuitry*. In this manner commercially available op-amps may be used in the circuitry preceding the AD9260 without dramatically degrading the noise performance of the system.

Common-Mode Level

The CML pin is an internal analog bias point used internally by the AD9260. This pin must be decoupled to analog ground with at least a 0.1uF capacitor as shown in Figure XX4. The dc level of CML is approximately AVDD/2.5. This voltage should be buffered if it is to be used for any external biasing.

Note: the common-mode voltage of the input signal applied to the AD9260 need not be at the exact same level as CML. While this level is recommended for optimal performance, the AD9260 is tolerant of a range of input common-mode voltages around AVDD/2.5.

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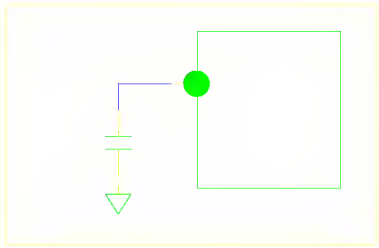

Figure 6: CML Decoupling

REFERENCE OPERATION

The AD9260 contains an on-board bandgap reference and internal reference buffer amplifier. The on-board reference provides a pin-strappable option to generate either a 1V or 2.5V output. With the addition of two external resistors, the user can generate reference voltages other than 1V and 2.5V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. See Table I. for a summary of the pin-strapping options for the AD9260 reference configurations.

Figure 7 shows a simplified model of the internal voltage reference of the AD9260. A pin-strappable reference amplifier buffers a 1V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. The voltage on the VREF pin determines the full-scale input span of the A/D. This input span equals,

Full-Scale Input Span = 1.6 × VREF

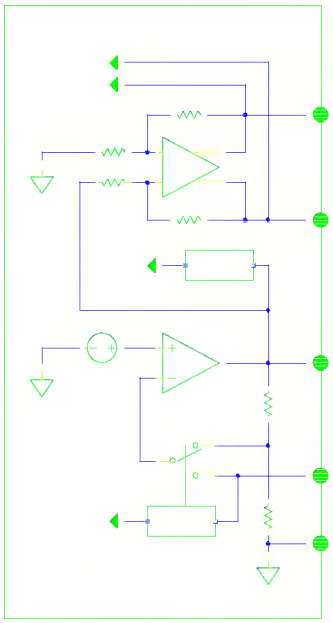

Figure 7: AD9260 Simplified Reference

The voltage appearing at the VREF pin as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains two comparators which monitor the voltage at the SENSE pin. The comparator with the lowest set point (approximately 0.3V) controls the position of the switch within the feedback path of A1. If the SENSE pin is tied to REFCOM, the switch is connected to the internal resistor network thus providing a VREF of 2.5V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch is connected to the SENSE pin. A short will provide a VREF of 1.0V while an external resistor network will provide an alternative VREF SPAN between 1.0V and 2.5V. The external resistor network may be implemented, for example, as a resistor divider circuit. This divider circuit could consist of a resistor (R1) connected between VREF and SENSE and another resistor (R2) connected between SENSE and REFCOM. The other comparator controls internal circuitry which will disable the reference amplifier if the SENSE pin is tied to AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

The reference buffer circuit, level shifts the reference to an appropriate common mode voltage for use by the internal circuitry. The on-chip buffer provides the low impedance necessary for driving the internal switched capacitor circuits and eliminates the need for an external buffer op-amp.

The actual reference voltages used by the internal circuitry of the AD9260 appear on the CAPT and CAPB pins. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple the CAPT and CAPB pins. Figure 8 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the A/D internal circuitry, (2) it provides the necessary compensation for A2, and (3) it bandlimits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15ms and should be evaluated in any power-down mode of operation.

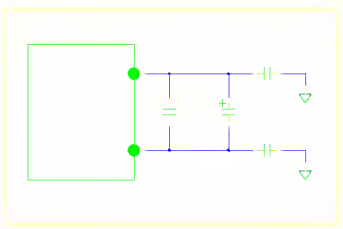

Figure 8: Recommend CAPT/CAPB Coupling Network

Reference Operating Mode	Input Span (VINA-VINB) (Vp-p)	Required VREF (V)	Connect	To
INTERNAL	1.6	1	SENSE	VREF
INTERNAL	4.0	2.5	SENSE	REFCOM
INTERNAL	$1.6 \leq SPAN \leq 4.0$ and $SPAN = 1.6 \times VREF$	$1 \leq VREF \leq 2.5$ and $VREF = (1+R1/R2)$	R1 R2	VREF & SENSE SENSE & REFCOM
EXTERNAL	$1.6 \leq SPAN \leq 4.0$	$1 \leq VREF \leq 2.5$	SENCE VREF	AVDD EXT. REF.

Table I. Reference Configuration Summary

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

The AD9260 output data is presented in a Two's Complement format. Table II. indicates the output data formats for various input ranges. A straight binary output data format can be created by inverting the MSB.

Input (V)	Condition (V)	Digital Output
VINA-VINB	< - 0.8*VREF	1000 0000 0000 0000
VINA-VINB	= - 0.8*VREF	1000 0000 0000 0000
VINA-VINB	= 0	0000 0000 0000 0000
VINA-VINB	= +0.8*VREF - 1LSB	0111 1111 1111 1111
VINA-VINB	>= + 0.8*VREF	0111 1111 1111 1111

Table II. Output Data Format (2X, 4X, 8X Decimation Mode)

The output data format in 1X decimation differs from that in 2X, 4X, and 8X decimation modes. In 1X decimation mode the output data remains in a Two's Complement format, but the digital numbers are scaled by a factor of 7/128. This factor of 7/128 is the product of internal scale factor of 7/8 in the analog modulator and a 1/16 scale factor caused by LSB justification of the 12-bit modulator data.

CSB AND READ PINS

The CSB and READ pins control the state of the output data pins (BIT1-BIT16) on the AD9260. The CSB pin is active low and the READ pin is active high. When CSB and READ are both active the ADC data is driven on the output data pins, otherwise the output data pins are in a high impedance (hi-Z) state. Table III. indicates the relationship between the CSB and READ pins and the state of pins BIT1-BIT16.

CSB	READ	Condition of Data Output Pins
Low	Low	Data output pins in hi-Z state
Low	High	ADC data on output pins
High	Low	Data output pins in hi-Z state
High	High	Data output pins in hi-Z state

Table III. CSB and READ Pin Functionality

DAV PIN

The DAV pin indicates when the output data of the AD9260 is valid. The rising edge of DAV may be used to latch the output data. The output data remains valid for at least 3.6ns after DAV rises as indicated in the AD9260 timing diagram (t_H = 3.6ns).

RESETB PIN

The RESETB pin is active low. When RESETB is asserted low the clocks in the digital decimation filters are disabled, the DAV pin goes low, and the data on the digital output data pins (BIT1-BIT16) is invalid. The RESETB pin also resets the state of the analog modulator in the AD9260 and resets the state of the internal clock dividers used in the decimation filters.

The state of the internal decimation filters in the AD9260 remains unchanged when RESETB is asserted low. Consequently, when RESETB is pulsed low, this resets the analog modulator but does not clear all the data in the digital filters. The data in the filters is corrupted by the effect of resetting the analog modulator (this causes an abrupt change at the input of the digital filter and this change is unrelated to the signal at the input of the A/D converter) For this reason, following a pulse on the RESETB pin, the decimation filters must be flushed of their data. These filters have a memory length which is equal to the product of the group delay of the filter times the clock rate of the converter. This memory length may be interpreted in terms of a number of samples stored in the decimation filter. For example, if the part is in 8X decimation mode, then the group delay is 345/fCLOCK. This corresponds to 345 samples stored in the decimation filter. These 345 samples must be flushed from the AD9260 after RESETB is pulsed low prior to re-using the data from the AD9260. That is, the AD9260 should be allowed to clock for 345 samples as the corrupted data is flushed from the filters. If the part is in 4X or 2X decimation mode then the relatively smaller group delays of the 4X and 2X decimation filters result fewer samples that must be flushed from the filters (109 samples and 23 samples respectively).

RESETB may be used to synchronize multiple AD9260s clocked with the same clock. The decimation filters in the AD9260 are clocked with an internal clock divider. The state of this clock divider determines when the output data becomes available (relative to CLK). In order to synchronize multiple AD9260s clocked with the same clock it is necessary that the clock dividers in each of the individual AD9260s are all reset to the same state. When RESETB is asserted low these clock dividers are cleared. The next rising edge of CLK following the rising edge of RESETB the clock dividers begin counting and the clock is applied to the digital decimation filters.

RESETB must be asserted for at least one entire period of CLK to insure that the internal clock dividers and the analog modulator are both reset. De-assertion of RESETB should occur on the falling edge of CLK (i.e. rising edge of RESETB should be coincident with falling edge of CLK)

OTR PIN

The OTR pin indicates that an over-range condition has occurred within the AD9260. An over-range condition must be handled carefully because of the group delays in the low-pass digital decimation filters in the output stages of the AD9260. When the input signal exceeds the full-scale range of the converter, this can have a variety of effects upon the operation of the AD9260 depending on the duration and amplitude of this over-range condition. A short duration over-range condition (<< filter group delay) may cause the analog modulator to briefly over-range without causing the data in the low-pass digital filters to exceed full-scale. The analog modulator is actually capable of processing signals slightly (3%) beyond the full-scale range of the AD9260 without internally clipping. A long duration over-range condition will cause the digital filter data to exceed full-scale. For this reason, the OTR signal is generated using two separate internal out-of-range detectors. The first of these out-of-range detectors is placed at the output of the analog modulator and indicates whether the modulator output signal has extended 3% beyond the full-scale range of the converter. If the modulator output signal exceeds 3% beyond full-scale then the digital data is hard-limited (i.e. clipped) to a number which is 3% larger than full-scale. The second out-of-range detecter is placed at the output of the stage 3 decimation filter and detects whether the low-pass filtered data has exceeded full-scale. When this occurs the filter output data is hard-limited to full-scale. The OTR signal is a logical OR function of the signals from these two internal out-of-range detectors. If either of these detectors produces an out-of-range signal then the OTR pin goes high and the data may be seriously corrupted.

If the AD9260 is used in a system which incorporates automatic gain control (AGC), then the OTR signal may be used to indicate that the signal amplitude should be reduced. This may be particularly effective for use in maximizing the signal dynamic range if the signal includes high-frequency components that occasionally exceed full-scale by a small amount. If, on the other hand, the signal includes large amplitude low-frequency components that cause the digital filters to over-range then this may cause the low-pass digital filter to over-range. In this case the data may become seriously corrupted and the digital filters may need to be flushed. See the RESETB pin function description above for an explanation of the requirements for flushing the digital filters.

OTR should be sampled with the falling edge of CLK. This signal is invalid while CLK is HIGH.

MODE OPERATION

The Mode Select Pin (MODE) allows the user to select one of four available digital filter modes using a single pin. Each mode configures the internal decimation filter to decimate at: 1X, 2X, 4X, or 8X. Refer to table IV. for mode pin ranges.
The mode selection is performed by using a set of internal comparators, as illustrated in figure 9, so that each mode corresponds to a voltage range on the input of the MODE pin. The output of the comparators are fed into encoding logic where, on the falling edge of the clock, the encoded data gets latched.

MODE PIN RANGE	TYPICAL MODE PIN	DECIMATION MODE
0V - 0.5V	GND	8X
0.5V - 1.5V	VREF/2	2X
1.5V - 3.0V	CML	4X
3.0 V - 5.0V	AVDD	1X

Table IV. Recommended Mode Pin Ranges and Configurations

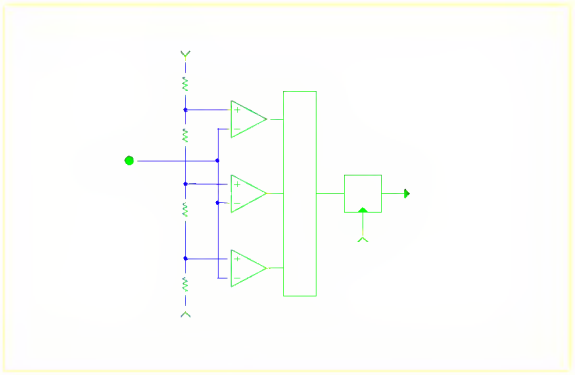

Figure 9: AD9260 Simplified Mode Pin Circuitry

BIAS PIN OPERATION

The Bias Select Pin (BIAS) gives the user, who is able to operate the AD9260 at a slower clock rate, the added flexibility of running the device in a lower, power consumption mode when it is clocked at less than 20MHz.
This is accomplished by scaling the bias current of the AD9260 as illustrated in figure 10. The Bias-amplifier drives a source follower and forces 1V across R_{ext}, which sets the bias current. This effectively adjusts the bias current in the modulator amplifiers and FLASH pre-amplifiers.When a large value of Rext is used, a smaller bias current is available to the internal amplifier circuitry. As a result these amplifiers need more time to settle, thus dictating the use of a slower clock as the power is reduced.
The scaling is accomplished by properly attaching an external resistor to the BIAS pin of the AD9260 as shown in table (BIAS). Rext is normally 2k ws for a clock speed of 20MHz and scales inversely with clock rate. Because BIAS is an external pin, minimization of capacitance to this pin is recommended in order to prevent instability of the bias pin amplifier.

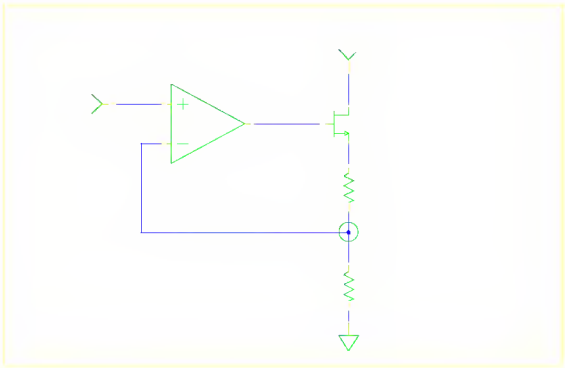

Figure 10: AD9260 Simplified Bias Pin Circuitry

AD9260 EVALUATION BOARD

GENERAL DESCRIPTION:

The AD9260 Evaluation Board was designed to provide an easy and flexible method of exercising the AD9260 and demonstrate it's performance to data-sheet specifications. The evaluation board is fabricated in four layers: the component layer; the ground layer ; the power layer and the solder layer. The board is clearly labeled to provide easy identification of components. Ample space is provided near the analog and clock inputs to provide additional or alternate signal conditioning.

FEATURES AND USER CONTROL:

- **Jumper Controlled Mode/OSR Selection:** The choice of Mode/OSR can be easily varied by jumping either JP1, 2, 3 or 4 as illustrated in figure 11 within the Mode/OSR Control Block. To obtain the desired Mode refer to table V.

Mode/OSR	Connect Jumper
1X	JP4
2X	JP2
4X	JP3
8x	JP1

Table V. AD9260 Evaluation Board Mode Select

- **Selectable Power Bias:** The power consumption of the AD9260 can be scaled down if the user is able to operate the device at a lower clock frequency. As illustrated in figure 11, pin-cups are provided for the external resistor (R2) tied to the BIAS pin of the AD9260. Table VI. defines the recommended resistance for a given clock speed to obtain the desired power consumption.

Resistor Value	Clock Speed (max)	Power Consumption
2KΩ	20MHz	550mW
4KΩ	10MHz	325mW
8KΩ	5MHz	200mW
16KΩ	2.5MHz	150mW

Table VI. AD9260 Evaluation Board Recommended Resistance Value for External Bias Resistor

- **Data Interfacing Controls:** The data interfacing controls (RESETB, CSB, READ, DAV) are all accessible via SMA connectors (J2 - J5) as illustrated in figure 11 within the Data Interfacing Control Block. The RESETB, CSB and READ connections are each supplied with two sets or resistor pin-cups to allow the user to pull-up or pull-down each signal to a fixed state... R5, R6 & R30 will terminate to Ground, while R7, R28 & R29 terminate to DRVDD. The DAV & OTR signals are also directly connected to the data output connector P1. All Interfacing Controls are buffered through the CMOS line driver 74HC541.

- **Buffered Output Data:** The 2's complement output data is buffered through two CMOS non-inverting bus transceivers (U2 & U3) and made available at pin connector P1 as illustrated in figure 11 within the Data Output Block.

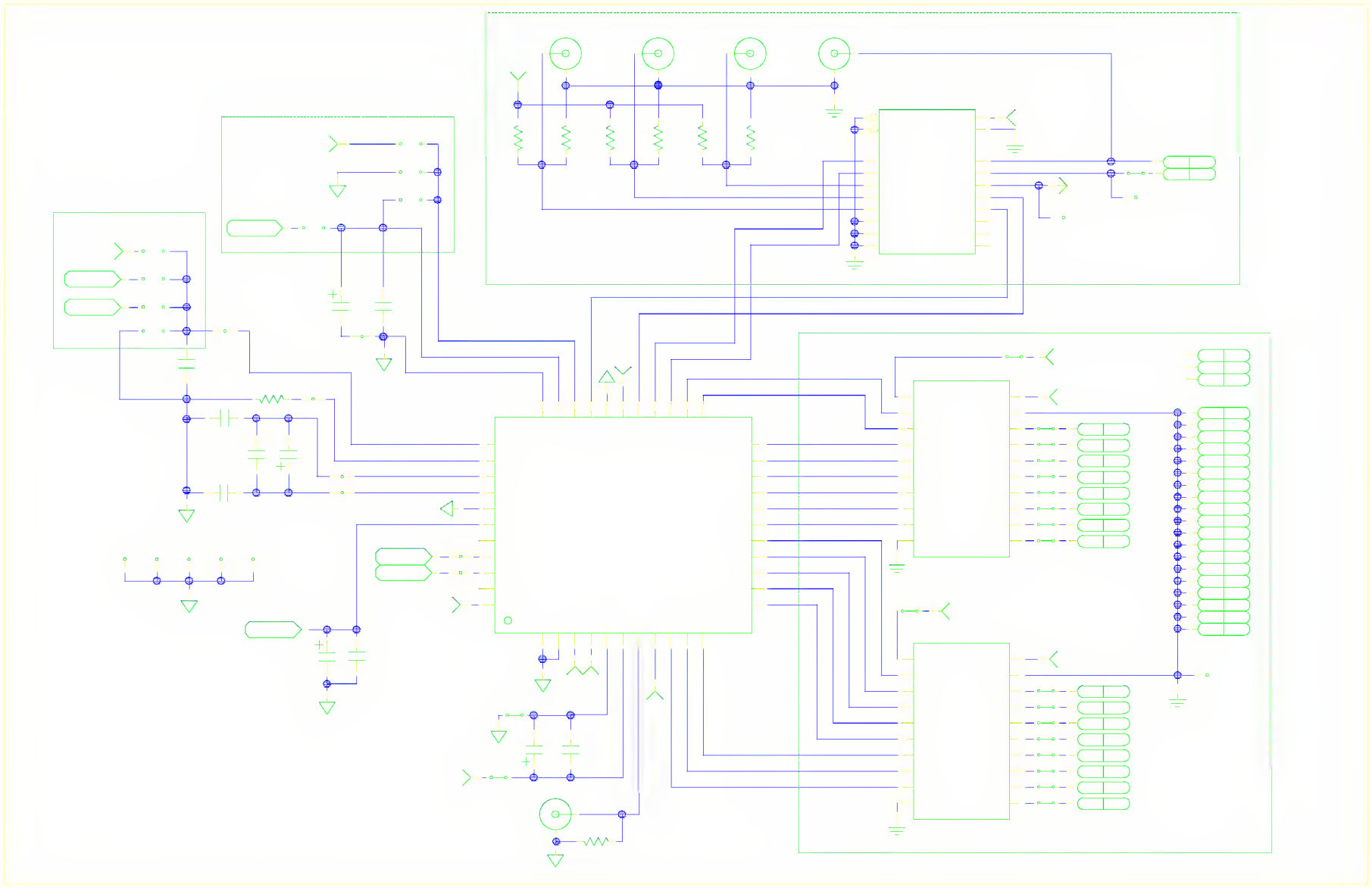

Figure 11: AD9260 Evaluation Board Top Level Schematic

- **Jumper Controlled Reference Source:** The choice of reference for the AD9260 can be easily varied between 1.0V, 2.5V or External, by using jumpers JP5, JP6, JP7 and JP9 as illustrated in figure 11 within the Reference Configuration Block. To obtain the desired reference see table VII.

Reference Voltage	Connect Jumper	Input Voltage (pk-pk FS)
2.5V	JP7	4.0V
1.0V	JP6	1.6V
External	JP5, JP9 & JP10	4.0V

Table VII. Ad9260 Evaluation Board Reference Pin Configuration

The External Reference circuitry, is illustrated in figure12. By connecting or disconnecting JP10, the External Reference can be configured for either 1.0V or 2.5V. That is, **by connecting JP10**, the external reference will be configured to provide a 2.5V reference. By **leaving JP10 open**, the external reference will be configured to provide a 1.0V reference.

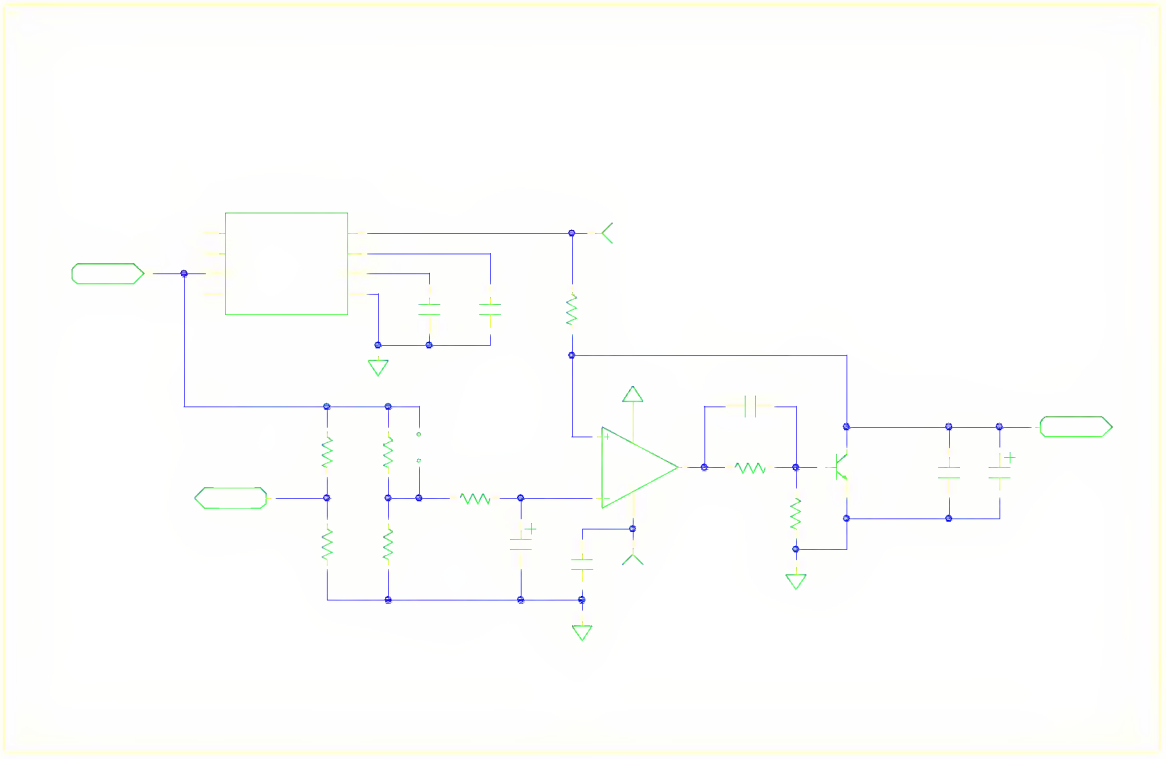

Figure 12: AD9260 Evaluation Board External Reference Circuitry

- **Selectable Input Signal Paths:** The AD9260 Evaluation Board allows the user to choose one of two input signal paths to the AD9260 as illustrated by figure 13. The DC_Input (J6) uses op-amp circuitry to generate a differential input to the device and demonstrates superior THD over a wider bandwidth. The AC_Input (J7) implements a buffered transformer as the input structure. The AC_Input will demonstrate superior SNR performanc, but sacrifices THD performance at lower input frequencies. Both input paths are fed through the Input Signal Driver illustrated in figures 13 & 14. This structure isolates any kick-

back, generated form the AD9260 inputs, from the Input Signal Conditioning Circuitry.

- **Selectable Input Signal Common Mode Level Source:** The input signals common mode level (CML) can be set by the AD9260's CML pin or generated by U10.

- **Selecting the DC_Input (J6) as the Input Signal Source:**
  1. Place jumpers across JP16 & JP17.
  2. Remove resistor RX2 and the Transformer (T1) from it's socket.
  3. Select which Input Signal Common Mode Level to use: Connect jumpers across JP11 & JP12 and remove resistor RX4 to use the AD9260's CML or remove JP11 & JP12 and connect resistor RX4 & RX3 to us the CML generated by U10. The CML generated by U10 is adjustable by using the 1KΩ trim-pot R35.
  4. The evaluation board is now ready to receive an input signal to the DC_Input (J6).

- **Selecting the AC_Input (J7) as the Input Signal Source:**
  1. Remove jumpers JP16 & JP17.
  2. Install or short, capacitor CX1 and resistor RX1.
  3. Insert Transformer (T1) into its socket.
  4. Select which Input Signal Common Mode Level to use: Connect jumper across JP12 and remove resistor RX4 & JP11 to use the AD9260's CML or remove JP12 and connect resistor RX4 & RX3 and jumper JP11 to us the CML generated by U10. The CML generated by U10 is adjustable by using the 1KΩ trim-pot R35.
  5. The evaluation board is now ready to receive an input signal to the AC_Input (J7).

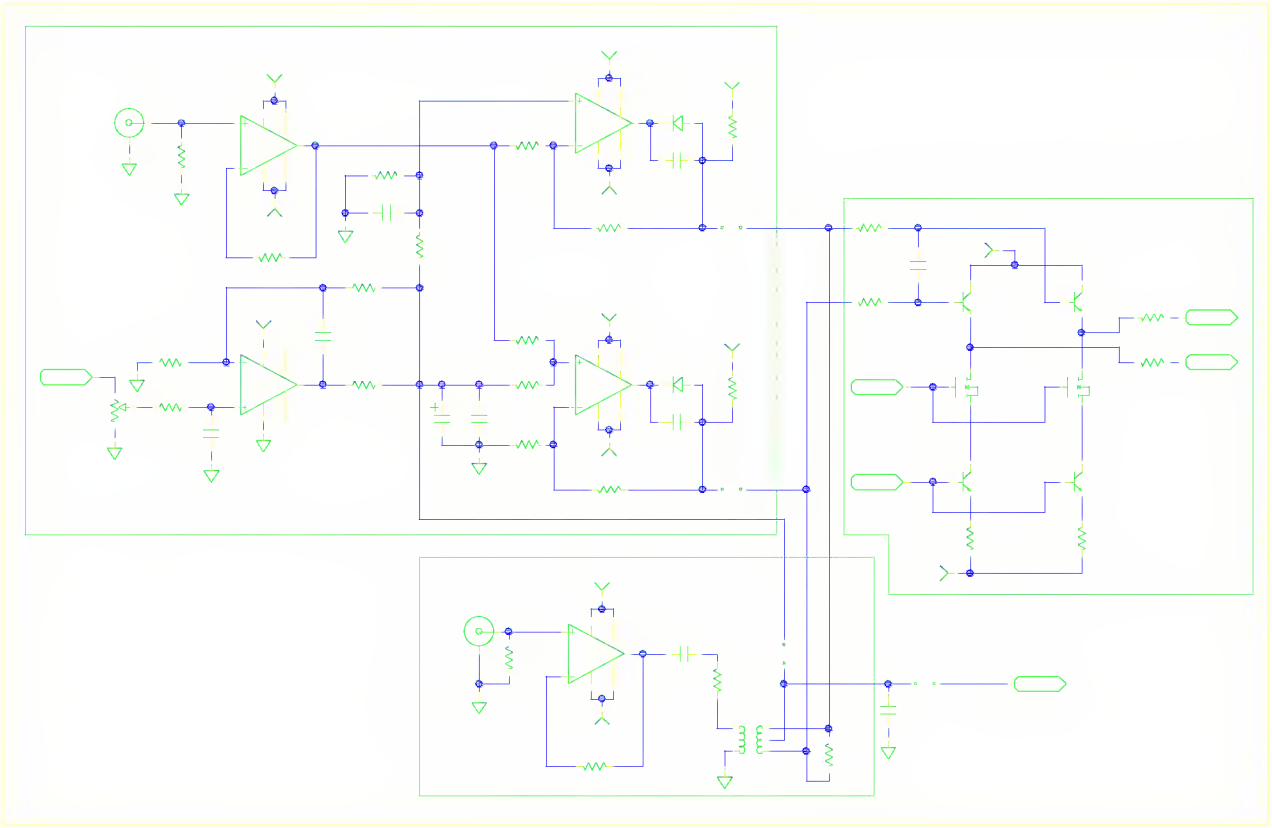

Figure 13: AD9260 Evaluation Board Input Configuration Block

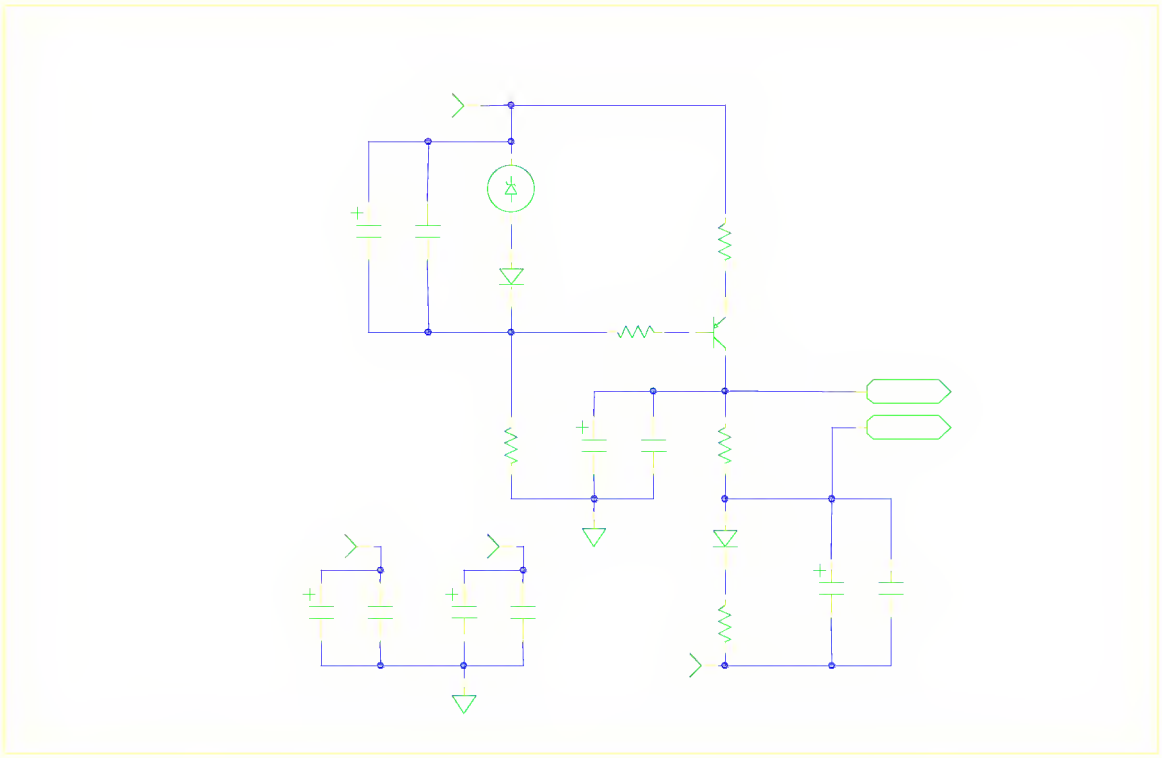

Figure 14: AD9260 Evaluation Board Bias Generator for Input Signal Driver

SHIPMENT CONFIGURATION AND QUICK SETUP

- **The AD9260 Evaluation Board is configured as follows when shipped:**

1. 2.5V External Reference/4.0V Differential Full-Scale Input : JP5, JP9 & JP10 connected, JP6 & JP7 disconnected.
2. 8X Mode/OSR: JP1 connected, JP2, JP3, & JP4 disconnected.
3. Full Speed Power Bias: R2 = 2kΩ and connected.
4. CSB pulled low: R6 = 49.9Ω and connected, R29 disconnected.
5. RESETB pulled high: R7 = 10kΩ and connected, R30 disconnected.
6. READ pulled high: R28 = 10kΩ and connected, R5 disconnected.
7. DC_Input Selected: JP16 & JP17 connected. Resistor RX2 & Transformer (T1) disconnected.
8. Input Signal Common Mode Level set by Trim-pot R35 to 1.8V: jumpers JP12 & JP11are disconnected and resistors RX4 & RX3 are connected.

QUICK SETUP:

1. Connect the required power supplies to the Evaluation Board as illustrated in figure15:
   - ⇒ +/-15VA supplies to P5 - Analog Power
   - ⇒ +5VA supply to P4 - Analog Power
   - ⇒ +5VD supply to P3 - Digital Power
   - ⇒ +5VD supply to P2 - Driver Power
2. Connect a Clock Source to CLKIN (J1): Note: 50Ω terminated by R1.
3. Connect an Input Signal Source to the DC_Input (J6).
4. Turn Power On!
5. The AD9260 Evaluation Board is now ready for use.

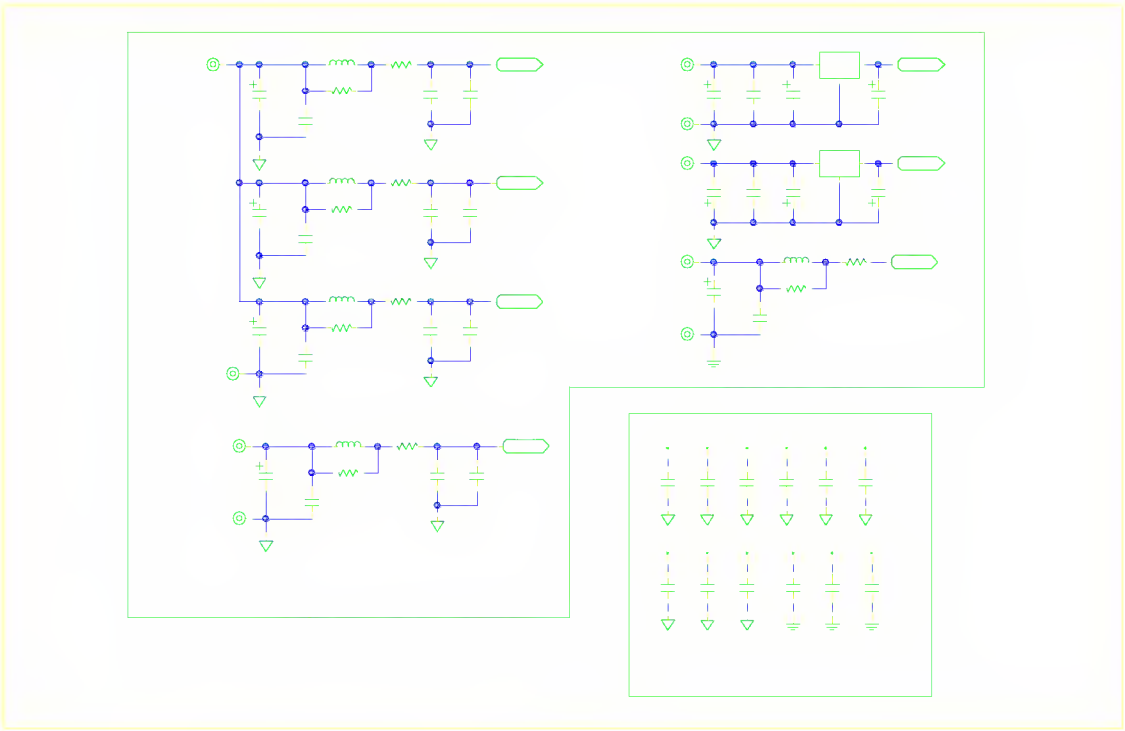

Figure 15: AD9260 Evaluation Board Power Supply configuration and Coupling

APPLICATION TIPS

1. The ADC analog input should not be over-driven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not over-range the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than -6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or band-pass filtering) of test signal generators is absolutely necessary for THD and IMD tests.
4. Test signal generators must have exceptional noise performance to achieve accurate SNR measurements. Good generators together with fifth-order elliptical band-pass filters are recommended for SNR tests. Narrow bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high signal levels.
5. The analog inputs of the AD9260 should be terminated directly at the input pin sockets with the correct filter terminating impedence (50Ω or 75Ω), or it should be driven by a low output impedance buffer. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance particularly at higher input frequencies. A high-frequency generator, based upon a clock source (e.g. crystal source), is recommended. Frequency-synthesized clock generators should generally be avoided because they typically provide poor jitter performance. See Note 8 if a crystal-based clock generator is used during FFT testing.

   A low jitter clock may be generated by using a high-frequency clock source and dividing this frequency down with a low-noise clock divider to

obtain the AD9260 input CLK. Maintaining a large-amplitude clock signal may also be very beneficial in minimizing the effects of noise in the digital gates of the clock generation circuitry.

Finally, special care should be taken to avoid coupling noise into any digital gates peceding the AD9260 CLK pin. Short leads are necessary to preserve fast rise times and careful decoupling sould be used with these digital gates and the supplies for these digital gates should be connected to the same supplies as that of the intenal AD9260 clock circuitry (pins 44 & 38).

7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies.
9. A well-designed, clean PC board layout will assure proper operation and clean spectral response, Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multi-layer PC boards are recommended for best performance, but a two-sided PC board with large heavy (20oz-foil) ground planes can give excellent results, if carefully designed.
10. Prototype "plug-boards" or wire-wrap boards will not be satisfactory.